Exhibit A – Part 1

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES S.A. and SOITEC USA, INC., Plaintiffs and Counterclaim Defendants, v. MEMC ELECTRONIC MATERIALS, INC. Defendant and Counterclaim Plaintiff.	**JURY TRIAL DEMANDED** Civil Action No.: 1:05-cv-00806-KAJ

FIRST AMENDED COMPLAINT
FOR DECLARATORY JUDGMENT

Plaintiffs S.O.I.TEC Silicon On Insulator Technologies S.A. and Soitec USA, Inc. (collectively, "SOITEC"), for their complaint for declaratory judgment against Defendant MEMC Electronic Materials, Inc. ("MEMC"), allege as follows that United States Patent No. 6,236,104 (the "'104 Patent") is invalid, unenforceable, and/or not infringed by SOITEC.

THE PARTIES

1. S.O.I.TEC Silicon On Insulator Technologies S.A., established in 1992, is the leading technology developer and manufacturer of silicon-on-insulator ("SOI") semiconductor wafers and other engineered substrates used in the electronics industry. SOITEC's unique proprietary technologies include its patented Smart Cut™ process and

its patented UNIBOND™ SOI wafers. SOITEC's technological innovations have resulted in the award of over 100 patents worldwide.

2. S.O.I.TEC Silicon On Insulator Technologies S.A. is organized as a Societé Anonyme under the laws of France and has a principal place of business in Bernin, France.

3. Soitec USA, Inc., a wholly-owned subsidiary of S.O.I.TEC Silicon On Insulator Technologies S.A., is a corporation organized under the laws of the Commonwealth of Massachusetts and has a principal place of business in Peabody, Massachusetts.

4. On information and belief, MEMC is a corporation organized and existing under the laws of the State of Delaware and has a principal place of business in St. Peters, Missouri.

JURISDICTION AND VENUE

5. This action arises under the Patent Laws of the United States. 35 U.S.C. §1 et seq.

6. This Court has jurisdiction over the subject matter of these claims under 28 U.S.C. §§1331, 1338(a), 2201, and 2202.

7. Venue is proper in this judicial district under 28 U.S.C. §§1391(b) and 1391(c).

FACTS COMMON TO ALL COUNTS

8. SOITEC develops and manufactures semiconductor products, including silicon-on-insulator structures. Since at least 1996 SOITEC has made these semiconductor products exclusively at its manufacturing facility in Bernin, France and

sold them in the United States. SOITEC continues to make these semiconductor products and sell them in the United States.

9. By letter dated October 15, 2004 (attached as Exhibit 1), MEMC, by its Senior Vice President of Research and Development, Dr. Shaker Sadasivam, inquired of Mr. Emmanuel Huyghe, SOITEC's Industrial Property Manager, as to why SOITEC's semiconductor products and their preparation fell outside of MEMC's alleged patent estate, including U.S. Patents Nos. 5,919,302; 6,236,104; 6,254,672; 6,287,380; and 6,342,725.

10. U.S. Patent No. 6,409,827 ("the '827 patent") was issued to MEMC on June 25, 2002, and is a continuation of U.S. Patent No. 6,287,380. The '827 patent claims priority to the same application as U.S. Patent Nos. 5,919,302; 6,254,672; and 6,287,380, was issued subject to a terminal disclaimer as to the portion of its term, and is substantially the same as U.S. Patent No. 6,287,380.

11. Subsequent to MEMC's October 2004 letter, U.S. Patent No. 6,849,901 ("the '901 patent") was issued to MEMC. The '901 patent claims priority to the same applications as U.S. Patent Nos. 6,236,104 and 6,342,725, and it was issued subject to a terminal disclaimer as to the portion of its term extending beyond the life of those patents.

12. In correspondence to SOITEC including a letter dated October 21, 2005 (attached as Exhibit 2) MEMC, by its Vice President and General Counsel, Bradley D. Kohn, accused SOITEC of past and continuing infringement of MEMC's intellectual property and requested a response by November 15, 2005.

13. In a November 8, 2005 phone call and subsequent email (attached as Exhibit 3), SOITEC, by its General Counsel Jacques-Elie Levy, responded to the letter dated October 21 and offered to travel to MEMC's principal place to meet with MEMC to discuss MEMC's allegations of infringement.

14. In an email dated November 18, 2005 (attached as Exhibit 4), MEMC, by its Vice President and General Counsel, Bradley D. Kohn, advised Mr. Levy that the contemplated meeting would be futile unless SOITEC were "to arrive with a specific proposal that addresses how SOITEC intends to remedy what we [MEMC] believe is significant past infringement and continuing infringement." Mr. Kohn declined to meet to "debate" whether or not SOITEC was infringing the MEMC patents, and stated that, "There are more appropriate forums in which to have that debate."

15. As a result of the communications culminating in the email of November 18, 2005, SOITEC was in fear and apprehension that MEMC would commence action against SOITEC for infringement at least of U.S. Pat. Nos. 5,919,302; 6,236,104; 6,254,672; 6,287,380; 6,342,725; 6,849, 901; and 6,409,827, and commenced this suit seeking a declaration of invalidity and noninfringement as to each of the foregoing patents by filing its Complaint on November 21, 2005.

16. Since the filing of the suit, the parties have been able to come to an agreement regarding MEMC's right to assert U.S. Patents No. 5,919,302; 6,254,672; 6,287,380; 6,342,725; 6,849, 901; and 6,409,827, and by reason of that agreement, SOITEC no longer seeks any declaratory relief as to those patents. No agreement has been reached with respect to the '104 Patent. MEMC has filed a counterclaim in this

case alleging that SOITEC infringes the '104 Patent and seeking damages and injunctive relief for said alleged infringement.

17. On information and belief, MEMC is the assignee and owner of the '104 patent, a copy of which attached hereto as Exhibit 5.

18. As a result of the aforementioned correspondence, and based on the threats made therein, SOITEC, at the time this suit was commenced, had a reasonable fear and apprehension that MEMC would commence an action against it in the United States for infringement of the '104 patent. SOITEC continues to have a reasonable fear and apprehension that MEMC will commence an action against it in the United States for infringement of the '104 patent.

19. An actual and justiciable controversy therefore exists between the parties.

COUNT I

DECLARATION OF NONINFRINGEMENT

20. SOITEC realleges and incorporates herein by reference the allegations set forth in paragraphs 1-19.

21. SOITEC does not infringe any valid claim of the '104 patent.

COUNT II

DECLARATION OF INVALIDITY

22. SOITEC realleges and incorporates herein by reference the allegations set forth in paragraphs 1-21.

23. One or more claims of the '104 patent are invalid for failure to comply with one or more of the conditions of. patentability set forth in 35 U.S.C. §§101, 102 and

103 and for failure to comply with one or more of the provisions of 35 U.S.C §§112 and 116.

COUNT III

DECLARATION OF CO-INVENTORSHIP

24. SOITEC realleges and incorporates herein by reference the allegations set forth in paragraphs 1-23.

25. MEMC's '104 patent claims and purports to disclose the invention of a silicon on insulator structure comprising, *inter alia*, "a single crystal silicon device layer having a central axis, a circumferential edge, a radius extending from the central axis to the circumferential edge, and a first axially symmetric region, in which there is a predominant intrinsic point defect, which is substantially free of agglomerated intrinsic point defects" (an "Agglomerate Free Device Layer"), a handle wafer, and an insulating layer between the handle wafer and the device layer. MEMC has consistently taken the position in various public pronouncements and in other lawsuits that essentially any Czochralski grown ("CZ") silicon wafer which is substantially free of crystal originated particle ("COP") defects has characteristics of the sort claimed for the Agglomerate Free Device Layer of the SOI structure claimed in the '104 Patent.

26. SOITEC manufactures its patented Unibond™ silicon on insulator product using its patented Smart Cut™ technology. SOITEC began the process of commercializing Smart Cut™ in 1995.

27. An early problem with Unibond™ SOI material made by the Smart Cut™ technique -- as well as with other SOI material made by fabrication techniques which

involved the transfer of a layer of silicon from one wafer to another -- was an excessive number of defects known as "HF defects" in the device layer of the final SOI structures.

28. During the Spring and early Summer of 1996, a number of researchers reported findings which indicated that, for SOI made using layer transfer techniques such as Smart Cut™, at least some HF defects were caused by the presence of tetrahedral agglomerated intrinsic point defects ("COP's") in the bulk CZ silicon wafers from which the SOI device layers were taken.

29. At the time the results linking COP's to HF defects became public, SOITEC and MEMC were in discussions concerning a possible commercial relationship which would have included, among other things, a substantial investment by MEMC in SOITEC, a license from SOITEC to MEMC of its intellectual property and know-how associated with Smart Cut™ and the manufacture of Unibond™ wafers, an ownership interest in SOITEC for MEMC, and a supply relationship whereby MEMC would supply SOITEC with a substantial portion of its principal raw material -- silicon wafers.

30. Upon learning of the possible link between COP's and HF defects, André-Jacques Auberton-Hervé, the chief executive officer of SOITEC, contacted Lawrence Falster, the sole named inventor on the '104 Patent and one of the leading material scientists at MEMC, to discuss possible strategies for eliminating HF defects in SOITEC's Unibond™ wafers.

31. On October 30, 1996, Auberton-Hervé and Falster, together with a number of other employees of SOITEC and MEMC, met to discuss how to address the HF defect problem. During the course of the meeting, Falster and Auberton-Hervé jointly conceived the idea of making silicon on insulator structures comprising a handle wafer,

an Agglomerate Free Device Layer, and an insulating layer between the handle wafer and the device layer.

32. Subsequent to the October 30, 1996, meeting, SOITEC and MEMC broke off their negotiations as to a potential business partnership, and, in 1997, SOITEC entered into such a partnership with Shin-Etsu Handotai ("SEH") a competitor of MEMC.

33. Subsequent to the October 30, 1996, meeting, under the direction of Auberton-Hervé, SOITEC diligently conducted extensive experiments using different types of starting device layer material and different treatments of its SOI device layer in an effort to control the HF defect problem.

34. Prior to the September 2, 1998, filing date for the provisional application to which the '104 Patent claims priority, SOITEC reduced to practice the fabrication of SOI wafers with device layers which were made of CZ silicon and which were substantially free of COP's.

35. To the extent that any patentable inventions are disclosed and claimed in the '104 Patent, André-Jacques Auberton-Hervé is a co-inventor of one or more of such inventions, and SOITEC is a co-owner of the '104 Patent.

COUNT IV

DECLARATION OF UNENFORCEABILITY

36. SOITEC realleges and incorporates herein by reference the allegations set forth in paragraphs 1-35.

37. The '104 patent is unenforceable due to MEMC's inequitable conduct and unclean hands as set forth more fully below.

38. The following facts were known to Robert Falster, the named inventor of the '104 Patent and/or one or more of the attorneys responsible for prosecuting the '104 patent, but withheld from the United States Patent and Trademark Office ("PTO") during the prosecution which led to the '104 Patent:

a. As is set forth more fully in Count III of this Declaratory Judgment Complaint, André-Jaques Auberton-Hervé was a co-inventor of one or more of the purported inventions claimed in the '104 Patent. Auberton-Hervé's co-inventorship was not disclosed to the PTO during the prosecution which led to the '104 Patent. Auberton-Hervé's co-inventorship was known at least to Falster, who jointly conceived with Auberton-Hervé one or more of the claimed invention during the meeting of October 30, 1996.

b. United States Patent No. 5,919,302 ("the '302 patent") was issued by the PTO on July 6, 1999, during the prosecution of the '104 Patent. The earliest application from which the '302 Patent can claim priority was filed on April 9, 1998. Neither the pendency of the application leading to the '302 Patent, nor the issuance of that patent was disclosed to the examiner of the application leading to the '104 Patent during the prosecution of the '104 Patent. Falster knew of the co-pendency and issuance of the '302 Patent because he was a named co-inventor on that patent. One or more of the attorneys responsible for the prosecution of the '104 Patent knew of the application for and the prosecution and issuance of the '302 Patent because both patents were prosecuted by the same attorney.

c. Prior to the date on which the application for the '104 Patent was filed, it was known in the silicon industry that there were multiple alternative ways to make a silicon wafer with at least a surface layer substantially free of agglomerated intrinsic point defects ("Prior Art Silicon"). These techniques included (i) the use of thermal treatments to dissolve or annihilate agglomerated intrinsic point defects in CZ silicon subsequent to their formation and (ii) the epitaxial deposition of a thin crystalline layer of silicon on the surface of a CZ silicon wafer. Falster knew of the existence of these techniques for making Prior Art Silicon. Falster also knew that the Prior Art Silicon produced by these techniques was substantially identical to the silicon (the "MEMC Silicon") produced by the technique (the "MEMC Technique") purportedly disclosed in the '302 and the '104 Patents. Falster knew of the substantial identity between the Prior Art Silicon and the MEMC Silicon, because this substantial identity is disclosed in the specification of the '302 Patent, of which Falster was a co-

inventor. One or more of the attorneys responsible for the prosecution of the '104 Patent had similar knowledge because both '104 and the '302 Patents were prosecuted by the same attorney. The substantial identity between the Prior Art Silicon and the MEMC Silicon was not disclosed to the examiner during the prosecution of the application that led to the '104 Patent.

39. The facts knowingly withheld from the PTO during the prosecution of the '104 Patent were material to the prosecution of that patent:

a. Auberton-Hervé's co-inventorship of one or more of the inventions claimed in the '104 patent was material to the prosecution of the '104 Patent. Section §116 of the Patent Act requires that the identity of each of the inventors is to be set forth in the application for a patent. Accordingly, a reasonable examiner, had he known of Auberton-Hervé's co-inventorship might have required Auberton-Hervé's addition as a named inventor on the '104 Patent.

b. The co-pendency of the application which led to the '302 Patent and the ultimate issuance of that patent were material to the prosecution of the '104 Patent. SOI structures, including SOI structures with device layers made from the agglomerate free Prior Art Silicon, were well known at the time the '104 Patent was applied for. The only arguable point of novelty in one or more claims of the '104 Patent is the substitution of MEMC Silicon for Prior Art Silicon as the device layer of a SOI structure. The '104 Patent's description of this purported point of novelty is taken almost verbatim from the specification of the '302 Patent. Hence, had he known of the '302 Patent and application, a reasonable examiner might have concluded that the '104 Patent disclosed nothing inventive beyond what was disclosed and claimed in the '302 Patent, and that the '104 Patent should have therefore have been rejected on obviousness-type double patenting grounds in light of the '302 Patent.

c. The substantial identity between Agglomerate Free Silicon and '302 Silicon was material to the prosecution of the '104 patent. Because one or more of the claims of the '104 Patent essentially covers an SOI structure with a device layer made of MEMC Silicon, and because it was known to make SOI with a device layer composed of Prior Art Silicon, a reasonable examiner, being informed as to the substantial identity of Prior Art Silicon to MEMC Silicon, might have concluded that one or more of the claims of the '104 patent should have been rejected pursuant to 35 U.S.C. §§102 and/or 103.

40. On information and belief, Falster and/or one or more of the attorneys responsible for prosecuting the '104 patent knowingly withheld material facts about Auberton-Hervé's co-inventorship with the intention of misleading the PTO.

a. SOITEC is informed and believes that during the pendency of the '104 Patent, MEMC issued a press release stating that it has been MEMC's intent since before the filing of the '104 application to create "an extensive and all encompassing patent domain on Perfect Silicon." Perfect Silicon is MEMC's trade name for the MEMC Material which purportedly used to form the Agglomerate Free Device Layer of the '104 Patent's SOI.

b. SOITEC is informed and believes that Auberton-Hervé's co-inventorship of the purported inventions claimed in the '104 Patent was knowingly withheld from the PTO in order to avoid giving SOITEC an ownership interest in the '104 Patent which would have jeopardized MEMC's "extensive and all encompassing patent domain on Perfect Silicon."

41. On information and belief, Falster and/or one or more of the attorneys responsible for prosecuting the '104 patent knowingly withheld material facts about the issuance of the '302 Patent, the co-pendency of the '302 application, and the substantial identity between Prior Art Silicon and MEMC Silicon with the intention of misleading the PTO.

a. Many selected portions of the application for the '104 Patent are verbatim identical to corresponding portions of the application for the '302 Patent. Additional portions of the two applications, while not verbatim identical, are substantively the same. For example, the description in the '104 Patent at Columns 14 to 21 is for the most part identical to the description at Columns 5 to 12 in the '302 Patent. Similarly, examples 7-12 in the '104 Patent are substantially identical to Examples 2-7 in the '302 Patent. Likewise, Figures 1-25 of the '302 Patent are identical to Figures 11-35 of the '104 Patent, and these figures are identically described in the respective specifications of the two patents. These identical portions of the two applications purport to describe the MEMC Technique for making MEMC Silicon. The only significant difference between the disclosures of the '302 and the '104 Patents insofar as they relate to MEMC Silicon, is the omission from the '104 Patent of the '302 Patent's disclosure that Prior Art Silicon is substantially identical to MEMC Silicon. On information and belief, the specification of the '302 Patent was selectively imported into the application for the '104 Patent to mislead the examiner as to the

patentability of one or more of the purported inventions claimed in the '104 application.

b. Falster and one or more of the attorneys prosecuting the '104 Patent took affirmative steps to conceal from the examiner the existence and co-pendency of the '302 Patent and the '302 Patent's disclosure as to the substantial identity between Prior Art Silicon and MEMC Silicon. These steps included failing to disclose the '302 patent or the co-pendency of the application that led to it to the examiner on the '104 application; deleting the pertinent portions of the '302 application from the sections that were otherwise incorporated verbatim into the '104 application; electing to file the '104 application as a new application instead of a continuation in part of the '302 application; and referencing but failing to provide the examiner with a copy of a PCT counterpart of the '302 application. On information and belief, these steps were taken to mislead the examiner as to the patentability of one or more of the purported inventions claimed in the '104 application.

c. Prior art references containing the information about SOI were submitted to the examiner for review during the prosecution of the '104 Patent. These included references which disclosed making SOI having epitaxial or heat treated device layers. These references were buried among dozens of less material references and, in many instances, their disclosure was misleadingly incomplete. In one case, for example, the reference was disclosed without any disclosure of its date of publication, which would have shown it to be prior art to the '104 application. In other instances, the references did not disclose that the silicon constituting such device layers would be agglomerate free and, thus, substantially identical to the MEMC Silicon. On information and belief, these references were disclosed in this misleading manner to deceive the examiner as to the patentability of one or more of the purported inventions claimed in the '104 application.

PRAYERS FOR RELIEF

WHEREFORE, SOITEC requests judgment against MEMC and respectfully prays that this Court enter orders that:

(a) Declare that the claims of the '104 Patent are invalid;

(b) Declare that SOITEC has not committed any act of direct and/or indirect infringement of the '104 Patent with respect to products that SOITEC makes, uses, imports into the United States, offers for sale, or sells;

(c) Declare that the '104 Patent is unenforceable;

(d) Enjoin MEMC, its agents, servants, employees and attorneys, and all those in active participation or privity with any of them, from charging SOITEC or its agents, distributors, or customers with infringement of the '104 Patent, from representing to others that SOITEC is liable for patent infringement of the '104 Patent, and from otherwise interfering in any way with SOITEC's manufacture, use, import into the United States, offer for sale, or sale of semiconductor materials;

(e) Find that this is an exceptional case, pursuant to 35 U.S.C. § 285 and that SOITEC be awarded its reasonable attorney's fees, expenses and costs in this action; and

(f) Grant SOITEC such other and further relief as the Court deems just and proper.

JURY TRIAL DEMANDED

Pursuant to Federal Rule of Civil Procedure 38, SOITEC demands a trial by jury on all issues so triable.

Dated: April 5, 2006

EDWARDS ANGELL PALMER & DODGE LLP

/s/ John L. Reed

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312.558.5600
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Exhibit 1

MEMC

TECHNOLOGY IS BUILT ON US

October 15, 2004

MEMC Electronic Materials, Inc.

501 Pearl Drive (City of O'Fallon)
Post Office Box 8
St. Peters, Missouri 63376 USA

Phone: 636-474-7336
Fax: 636-474-5158
www.memc.com

BY FEDERAL EXPRESS AND
FACSIMILE – 011-33-04-7692-7501

Mr. Emmanuel Huyghe
Industrial Property Manager
S.O.I.T.E.C.
Parc Technologique des Fontaines
38190 Bernin, France

Dear Mr. Huyghe:

This letter is in response to your letter of September 30, 2004.

Our understanding is that the patent claims to which you draw our attention have been found invalid, and they will remain invalid unless and until the patent is reissued. We further understand that each claim appearing in the reissue application was rejected upon one or more grounds on June 7, 2004 and that no response to this rejection has been filed; if one has been filed, please let us know.

Even if the claims are reissued as you contend, however, we believe the processes we are developing will fall outside the scope of any such reissue claims. If you disagree, please advise us as to the expected scope of your claims so that we may give your position full consideration. In particular, your letter suggests that any manufacture or sale of bonded SOI wafers, sSOI wafers, or other similar devices produced by layer transfer methods will infringe a patent that you may receive. Is it your contention that the claims you are pursuing are this broad? If so, please explain why, because we do not understand this to have been Soitec's position in the past. If not, please describe in more detail what you believe the issued claims will cover.

MEMC respects the valid patent rights of others and would never take any action it knew to infringe the valid patent rights of another. Accordingly, please provide the above requested information to enable us to better understand whatever rights you believe you may have in this technology.

Relatedly, we note from your website that your UNIBOND product is described as containing COP-free material (active and handle wafers). We also understand that you supply SOI wafers to certain customers whose specifications require a COP-free device layer. MEMC has an extensive patent estate concerning COP-free silicon ingots and wafers (*i.e.*, agglomerated intrinsic point defect-free material), *per se*, methods of preparing such ingots and wafers, and SOI substrates prepared from such materials. See, for example, our U.S. Patent Nos. 5,919,302; 6,236,104; 6,254,672; 6,287,380; and

Dr. Shaker Sadasivam
Senior Vice President,
Research and Development

6,342,725 and European Patent Nos. 972,094; 973,963; and 973,964. We are interested in obtaining further information concerning your UNIBOND product and whether, for example, you believe your UNIBOND product and its preparation fall outside the scope of our patent estate and, if so, why. If you determine that you are interested in using MEMC's patented technology, MEMC will consider a request to license this technology.

We look forward to your reply.

Very truly yours,

Shaker Sadasivam

Dr. Shaker Sadasivam

EXHIBIT 2

MEMC

TECHNOLOGY IS BUILT ON US

MEMC Electronic Materials, Inc.

501 Pearl Drive (City of O'Fallon)
Post Office Box 8
St. Peters, Missouri
63376 USA

Phone: 636-474-5000
Fax: 636-474-5111
www.memc.com

bkohn@memc.com

October 21, 2005

VIA FEDERAL EXPRESS

Andre-Jacques Auberton-Herve
Chief Executive Officer
S.O.I.TEC Silicon On Insulator Technologies
38190 Bernin
France

Re: MEMC PerfectSilicon™ Patents

Dear Mr. Auberton-Herve:

I am the Vice President and General Counsel of MEMC Electronic Materials, Inc. ("MEMC"). I am writing to you directly in connection with past correspondence between our two companies relating to MEMC's PerfectSilicon™ Patents with the hope that my letter to you will generate a timely response from Soitec. In particular, we have been awaiting a definitive response from Soitec to our initial letter to your company (or your counsel) about these patents for over a year.

Background

On October 15, 2004, Dr. Shaker Sadasivam, MEMC's Senior Vice President, Research and Development, in response to a September 30, 2004 letter from Emmanuel Huyghe of your company regarding a Soitec patent, sent Mr. Huyghe a letter asking Mr. Huyghe for a response in connection with eight of MEMC's United States and European patents in the "Perfect Silicon" area, including European patent EP-B-0 972 094 (the "'094 Patent"). A copy of this October 15, 2004 letter is attached hereto for your convenience.

On November 10, 2004, Patrick F. Murray of Winston & Strawn LLP, Soitec's outside counsel, responded to Dr. Sadasivam's October 15 letter on behalf of Soitec, and stated that Soitec was in the process of reviewing MEMC's referenced patents, and that it was Soitec's hope to have a response to MEMC by the end of 2004. A copy of Mr. Murray's November 10, 2004 letter is also attached hereto for your convenience.

Bradley D. Kohn
Vice President and
General Counsel

When we had not received any response from Soitec by March 2005, on March 7, 2005, Dr. Sadasivam sent another letter to Mr. Murray, asking when the promised Soitec response would be forthcoming. A copy of this March 7, 2005 letter is attached hereto for your convenience. To date, we still have not received a response from Soitec regarding these patents.

Recent Developments

Recently, MEMC received a favorable decision from the European Patent Office ("EPO") Opposition Division in connection with the '094 Patent, which '094 Patent was opposed by Sumitomo Mitsubishi Silicon Corporation. MEMC's '094 Patent pertains to Low Defect Density, Vacancy Dominated Silicon, which is used in the preparation, manufacture and sale of semiconductor grade single crystal silicon ingots and wafers. The '094 Patent is one of the many European patents that MEMC has in the "Perfect Silicon" area, certain of which patents were brought to the attention of Soitec as described above.

After an all day hearing on October 11, 2005 in Munich, Germany, the EPO Opposition Division upheld the validity of the '094 Patent as such patent relates to the preparation, manufacture and sale (and use) of wafers with a diameter of 200 mm or greater. Consistent with our belief that Soitec is aware of and concerned regarding its potential infringement of our patents, at least one representative of Soitec (Mr. Huyghe) attended the hearing in Munich. As we have indicated in our letters to Soitec in the past, we are concerned that Soitec has infringed and may be infringing our intellectual property, including, but not limited to, the '094 Patent, in connection with the use, manufacture and sale of Soitec's SOI wafers.

As you also know, in mid-September 2005 Forbes published an article about Soitec and Soitec's products. In particular, the last statement in that article caught our attention: "[t]he donor wafer can be reused ten times before it gets too thin." We believe that if that statement is true, then the donor wafer must be "Perfect Silicon." If the donor wafer is in fact "Perfect Silicon", then the use, manufacture and sale of this "Perfect Silicon" donor wafer infringes our intellectual property and patents.

Before we take any further appropriate action, we would like to understand how Soitec has believed it is justified in using and selling such products, and how Soitec proposes to address and remedy this situation. Given that over a year has passed since our initial correspondence about this, and Soitec's obvious awareness of the issue, we would appreciate a response from you no later than November 15, 2005.

I look forward to hearing from you or your appointed representative. Please feel to contact me to discuss further.

Sincerely,

Bradley D. Kohn
Vice President and General Counsel

cc: Patrick F. Murray, Winston & Strawn LLP (via facsimile and Federal Express)
Dr. Emmanuel Huyghe (via email and Federal Express)

EXHIBIT 3

> De : Jacques-Elie LEVY
> Envoyé : vendredi 11 novembre 2005 13:22
> À : 'BKohn@memc.com'
> Objet : MEETING WITH SOITEC
>
> Dear Mr. Kohn,
> Following our recent cordial telephone call, I confirm my intention to meet you in order to discuss with you about the last letter you sent us on October the 21st.
> If it is convenient for you, our IP team and me could be available on December the 2nd and will come at your office.
> The SOITEC> '> s attendees will be Emmanuel Huyghe (SOITEC IP Manager) and our two patent attorneys George W. Neuner (Edwards Angell Palmer & Dodge LLP), and Michael L. Brody (Winston & Strawn, LLP).
> Could you please be so kind as to confirm your availability as soon as possible in order to coordinate the (busy) agendas of our team?
> Cordialement/Best Regards,
> Jacques Elie LEVY
> SOITEC S.A.
> Legal Department
> Chemin des Franques
> Parc Technologique des Fontaines
> 38190 BERNIN - FRANCE
> Tel.: +33 (0)4 76 45 52 86
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> _____
>

>
> > <<Jacques Elie LEVY (Télécopie bureau).vcf>>

EXHIBIT 4

Brad Kohn
<BKohn@memc.com>

11/18/2005 12:33 PM

To: "Jacques-Elie LEVY" <jacques-elie.levy@soitec.fr>
cc: "Emmanuel HUYGHE" <emmanuel.huyghe@soitec.fr>, GNeuner@eapdlaw.com, "Brody, Michael" <MBrody@winston.com>
Subject: Re: TR: MEETING WITH SOITEC

Mr. Levy,
Thanks for your email note dated November 11, 2005. While we were initially encouraged by Soitec's November 8 proposal to meet with us to have a discussion about our allegations of Soitec infringement, I am sorry to say that we were disappointed with the Soitec list of proposed attendees for the proposed December 2, 2005 meeting. We were disappointed with the list because we believe the list is likely too short in that it does not appear to include senior executives with decision-making authority.

Let me be clear about what we believe the purpose of this meeting must be, in order to make the meeting worthwhile for MEMC: we expect Soitec to arrive with a specific proposal that addresses how Soitec intends to remedy what we believe is significant past infringement and continuing infringement. Based on your list of proposed attendees, we do not believe that Soitec's purpose for the meeting is to present MEMC with a legitimate, thoughtful substantive proposal to address what we believe is significant past and current infringement. If Soitec's purpose for the meeting is instead to show up in St. Peters and explain to us why Soitec is not infringing our intellectual property, then I would respectfully submit to you that the meeting will not be worth it from our perspective, and you should not waste your time flying to St. Louis for such a meeting. Instead, please just send us that information in writing by November 22, 2005 so that we may evaluate your position.

Candidly, and forgive me for the blunt statement, right now it appears to us that the proposed December 2 meeting is yet another stalling tactic by Soitec. The time for stalling is over. Soitec has been on notice of our allegations of infringement for over a year. Another meeting to debate that point with us is worthless to MEMC. There are more appropriate forums in which to have that debate. We believe that a meeting between MEMC and Soitec, should it occur, should be held to avoid such a forum, not just to delay or preview such a forum.

Again, we remain happy to meet with Soitec to receive a specific proposal that addresses how Soitec intends to remedy what we believe is significant past and current infringement. If that is not Soitec's intended purpose and agenda for the meeting, then there is no need to convene such a meeting. I look forward to hearing from you about this. If your response indicates that a meeting will be fruitful, I will work with people's schedules here to make it happen.

Regards,
Brad Kohn

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EXHIBIT 5

US006236104B1

(12) **United States Patent**
Falster

(10) **Patent No.: US 6,236,104 B1**
(45) **Date of Patent: *May 22, 2001**

(54) **SILICON ON INSULATOR STRUCTURE FROM LOW DEFECT DENSITY SINGLE CRYSTAL SILICON**

(75) Inventor: **Robert J. Falster**, Milan (IT)

(73) Assignee: **MEMC Electronic Materials, Inc.**, St. Peters, MO (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/387,288**

(22) Filed: **Aug. 31, 1999**

Related U.S. Application Data

(60) Provisional application No. 60/098,902, filed on Sep. 2, 1998.

(51) **Int. Cl.**[7] **H01L 29/06**; H01L 27/01; H01L 27/12; H01L 31/0392

(52) **U.S. Cl.** **257/618**; 257/347; 257/913

(58) **Field of Search** 257/347, 618, 257/913

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Primary Examiner—Ngân V. Ngô
(74) *Attorney, Agent, or Firm*—Senniger, Powers, Leavitt & Roedel

(57) **ABSTRACT**

The present invention relates to a silicon on insulator ("SOI") structure having a low defect density device layer and, optionally, a handle wafer having improved gettering capabilities. The device layer comprises a central axis, a circumferential edge, a radius extending from the central axis to the circumferential edge, and a first axially symmetric region which is substantially free of agglomerated intrinsic point defects. Additionally, the present invention is directed to such a SOI structure which has a Czochralski single crystal silicon handle wafer which is capable of forming an ideal, non-uniform depth distribution of oxygen precipitates upon being subjected to the heat treatment cycles of essentially any arbitrary electronic device manufacturing process.

40 Claims, 35 Drawing Sheets

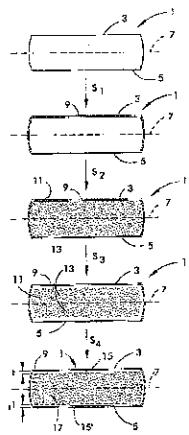

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FIG. 1

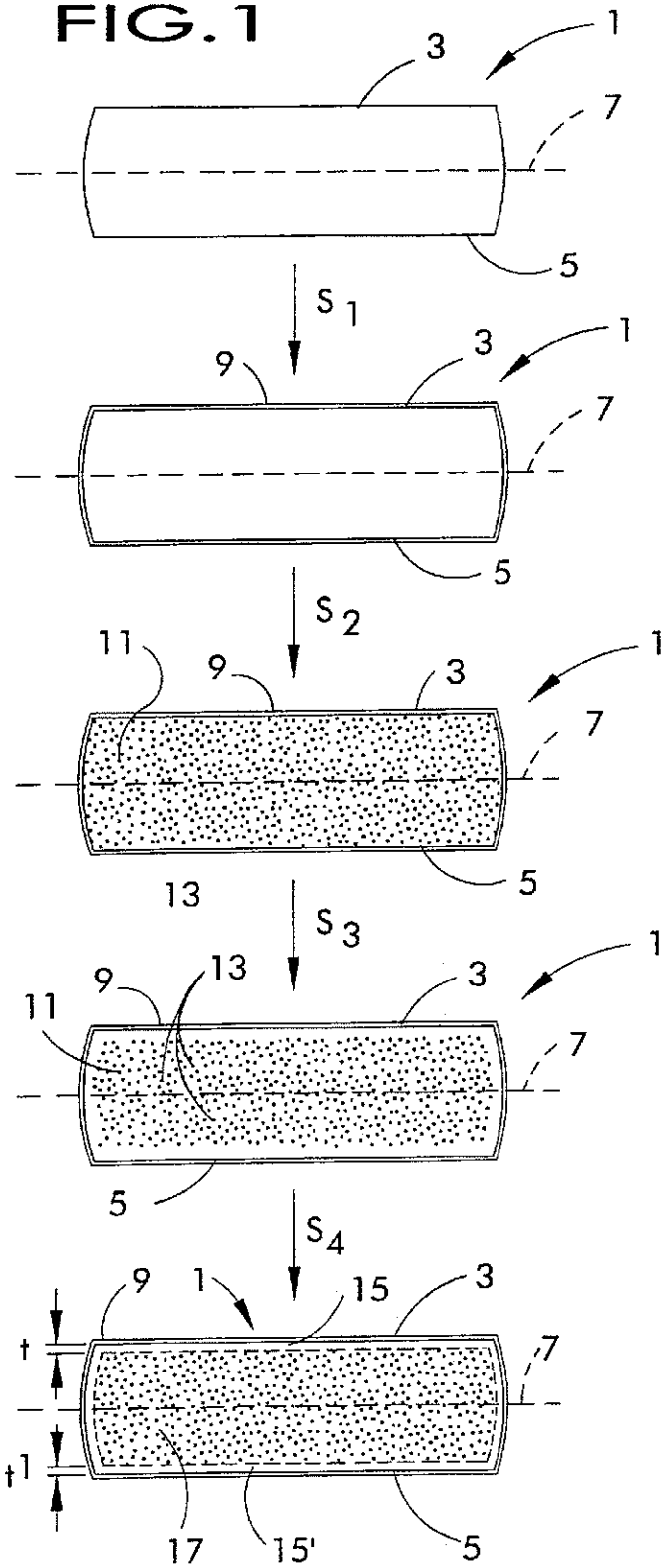

FIG.2

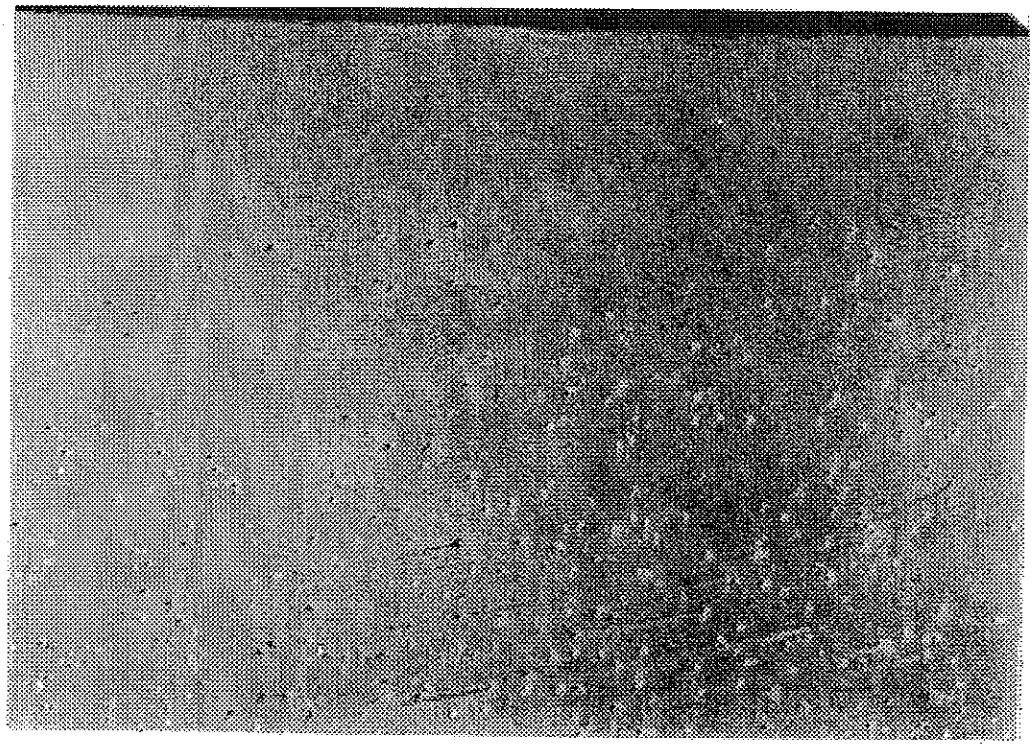

FIG 3

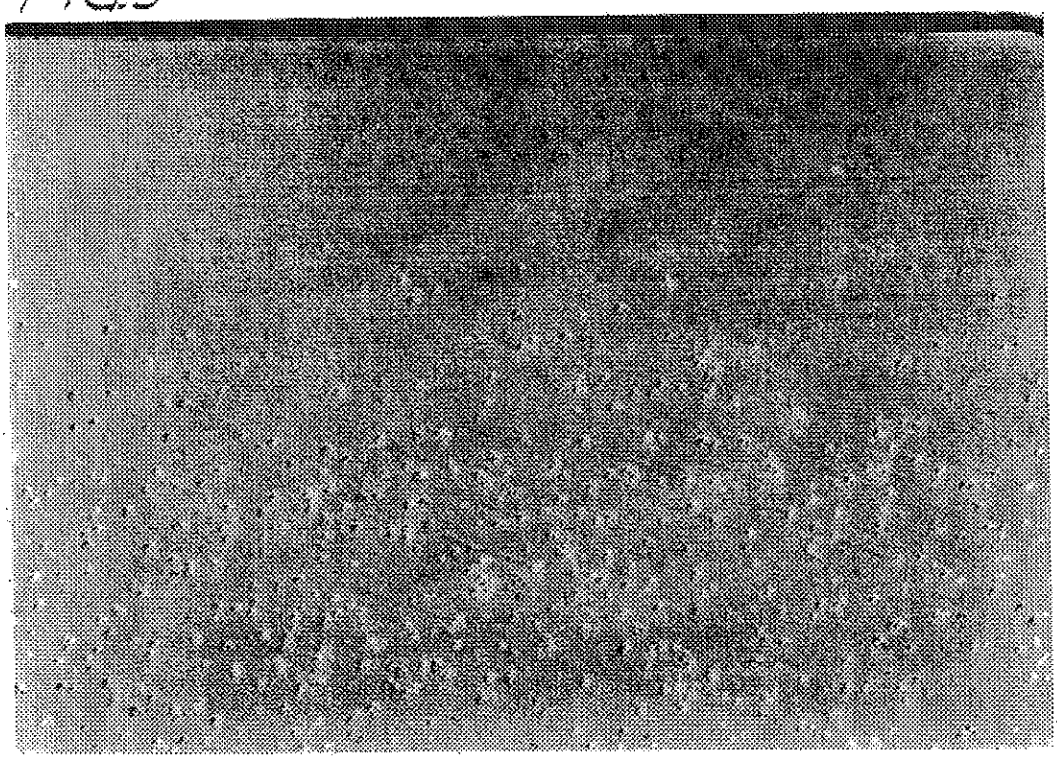

FIG.4

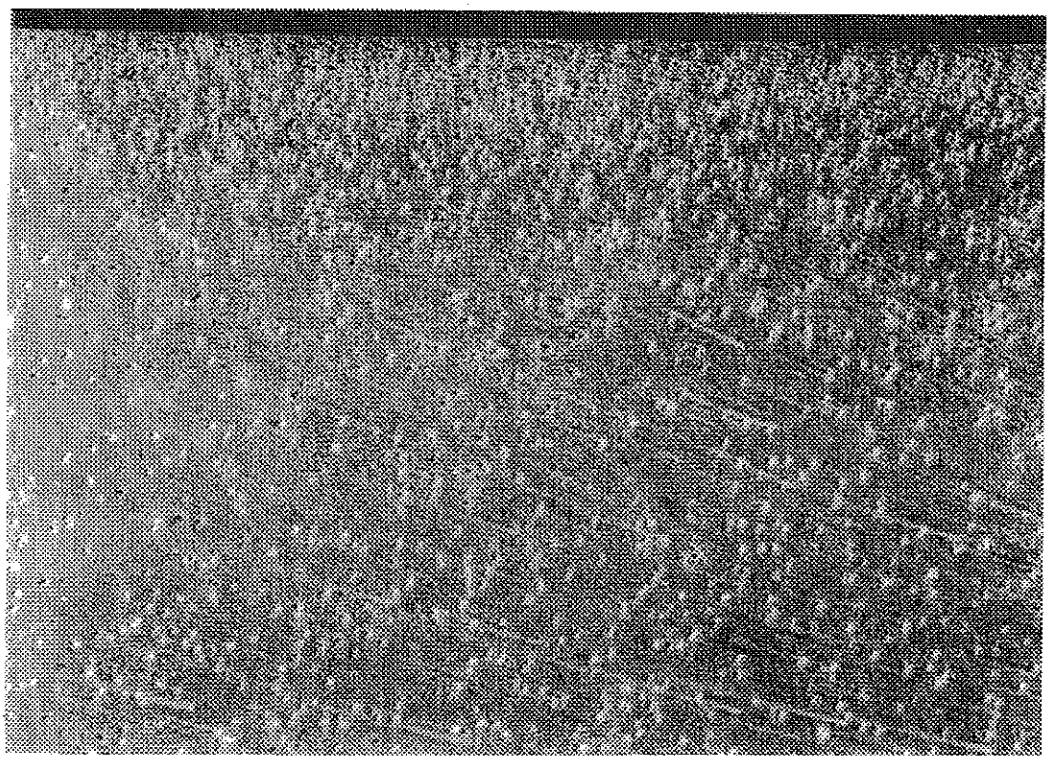

FIG. 5

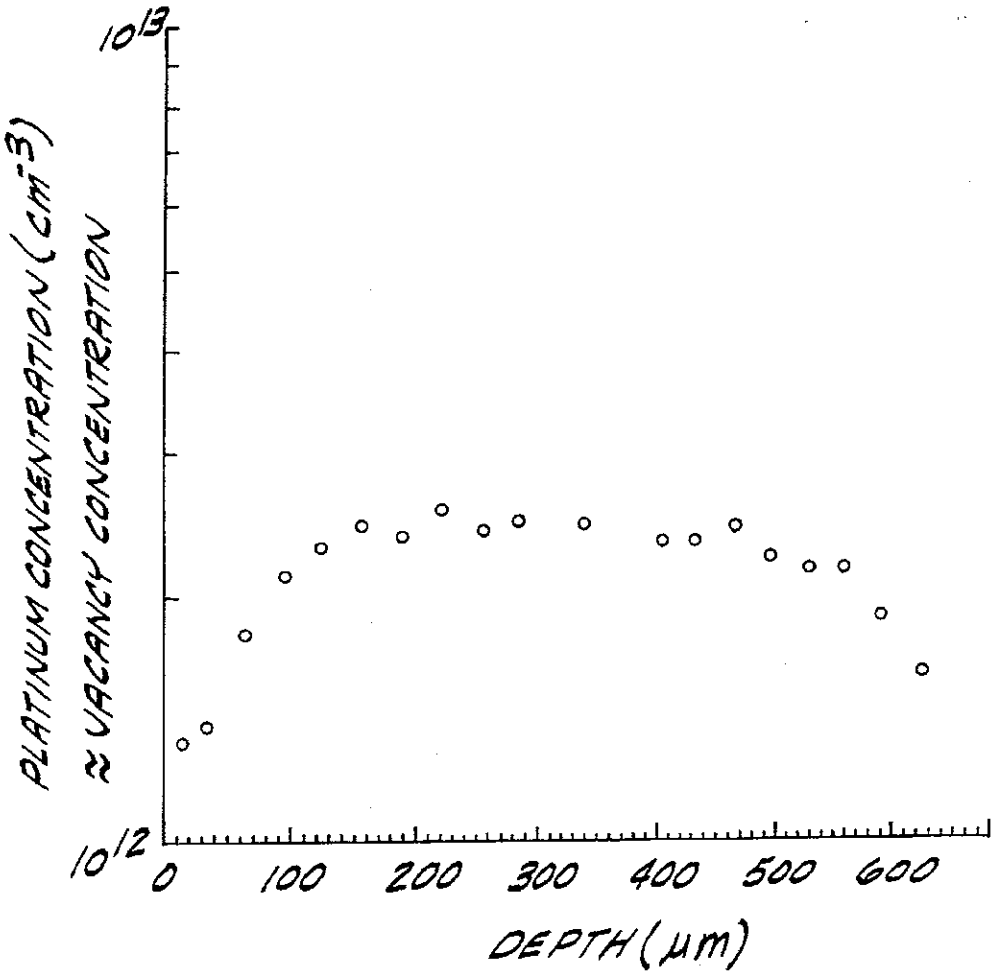
PLATINUM CONCENTRATION (cm-3)
≈ VACANCY CONCENTRATION
10^13
10^12
0
100
200
300
400
500
600
DEPTH (μm)

FIG 6

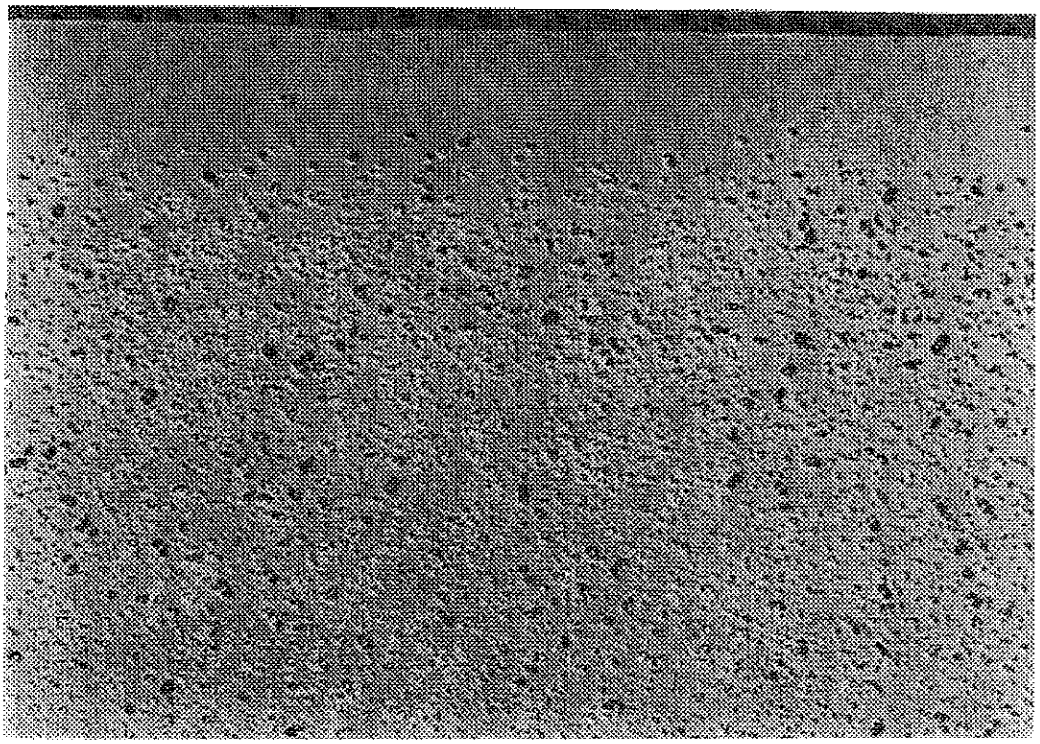

FIG. 7

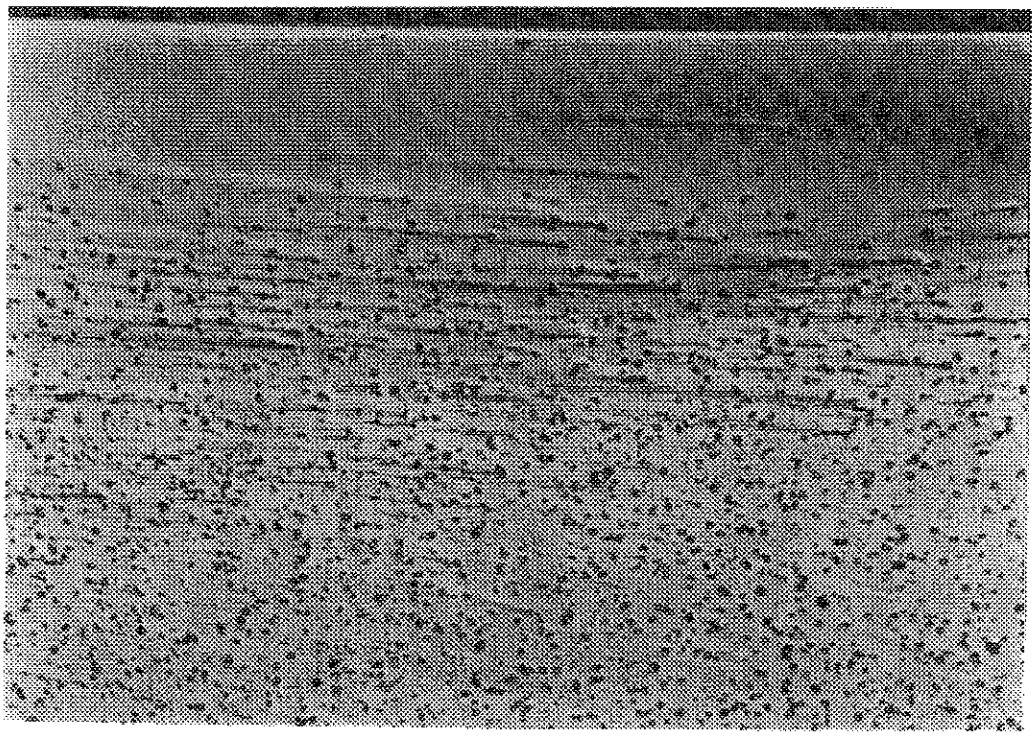

FIG.8